

WHAT IS CLAIMED IS:

1 1. A packet switch for switching cells comprising fixed-size
2 data packets, said packet switch comprising:

3 N input ports capable of receiving and storing cells in
4 a plurality of input queues;

5 N output ports capable of receiving and storing cells
6 from said N input ports in a plurality of output queues;

7 a switch fabric for transferring said cells from said N
8 input ports to said N output ports, said switch fabric comprising
9 an internally buffered crossbar having NxN internal buffers
10 associated therewith, wherein each internal buffer is associated
11 with a crosspoint of one of said N input ports and one of said N
12 output ports;

13 a scheduling controller capable of selecting a first one
14 of a plurality of queued head-of-line (HOL) cells from said input
15 queues to be transmitted to a first one of said NxN internal
16 buffers according to a fair queuing algorithm in which each of said
17 queued HOL cells is allocated a weight of R_{1j} and wherein said
18 scheduling controller is further capable of selecting a first one
19 of a plurality of HOL cells buffered in a second one of said NxN
20 internal buffers to be transmitted to a first one of said output
21 queues according to a fair queuing algorithm in which each of said

internally buffered HOL cells is allocated a weight of R_{ij} , wherein a group of K queues share a combined capacity of 1, and

$$\sum_{i=1}^K R_i \leq 1$$

where R_i is the guaranteed bandwidth associated with queue i , wherein any queue being non-empty over a time interval T can be guaranteed a bandwidth of $R_i T + E$, where E is a constant.

2. The packet switch as set forth in Claim 1 wherein said $N \times N$ internal buffers are disposed within said switch fabric.

3. The packet switch as set forth in Claim 1 wherein at least some of said $N \times N$ internal buffers are disposed within said N input ports.

4. The packet switch as set forth in Claim 1 wherein at least some of said $N \times N$ internal buffers are disposed within said N output ports.

1 5. The packet switch as set forth in Claim 1 wherein said
2 NxN internal buffers are configure within said N output ports such
3 that each output port has a fast internal speed-up of N output
4 buffer that is shared at least partially by cells from all input
5 ports.

1 6. A communication network comprising a plurality of packet
2 switches capable of transferring data in cells comprising fixed-
3 size packets, wherein at least one of said packet switches
4 comprises:

5 N input ports capable of receiving and storing cells in
6 a plurality of input queues;

7 N output ports capable of receiving and storing cells
8 from said N input ports in a plurality of output queues;

9 a switch fabric for transferring said cells from said N
10 input ports to said N output ports, said switch fabric comprising
11 an internally buffered crossbar having NxN internal buffers
12 associated therewith, wherein each internal buffer is associated
13 with a crosspoint of one of said N input ports and one of said N
14 output ports;

15 a scheduling controller capable of selecting a first one
16 of a plurality of queued head-of-line (HOL) cells from said input
17 queues to be transmitted to a first one of said NxN internal
18 buffers according to a fair queuing algorithm in which each of said
19 queued HOL cells is allocated a weight of R_{ij} and wherein said
20 scheduling controller is further capable of selecting a first one
21 of a plurality of HOL cells buffered in a second one of said NxN
22 internal buffers to be transmitted to a first one of said output

23 queues according to a fair queuing algorithm in which each of said
24 internally buffered HOL cells is allocated a weight of R_{ij} , wherein
25 a group of K queues share a combined capacity of 1, and

$$\sum_{i=1}^K R_i \leq 1$$

27 where R_i is the guaranteed bandwidth associated with queue i,
28 wherein any queue being non-empty over a time interval T can be
29 guaranteed a bandwidth of $R_i T + E$, where E is a constant.

1 7. The communication network as set forth in Claim 6 wherein
2 said NxN internal buffers are disposed within said switch fabric.

1 8. The communication network as set forth in Claim 6 wherein
2 at least some of said NxN internal buffers are disposed within said
3 N input ports.

1 9. The communication network as set forth in Claim 6 wherein
2 at least some of said NxN internal buffers are disposed within said
3 N output ports.

1 10. The communication network as set forth in Claim 6 wherein
2 said NxN internal buffers are configure within said N output ports
3 such that each output port has a fast internal speed-up of N output
4 buffer that is shared at least partially by cells from all input
5 ports.